Data Sheet

Orchestrating a brighter world NEC

Optimizing the Capacitor Layout by Visualization of Resonance Behavior Between the Power and GND

Power/ Ground Resonance Analysis

Overview

During the PCB layout design phase, reducing the resonance between the Power and GND, which is one of the dominant factors for EMI, can reduce rework after EMC test. This results in minimized design time and cost. In addition, arranging no more capacitors than necessary can reduce component cost.

The Power-GND Plane Resonance Analysis enables you to front-load EMI countermeasures, and has the following effects:

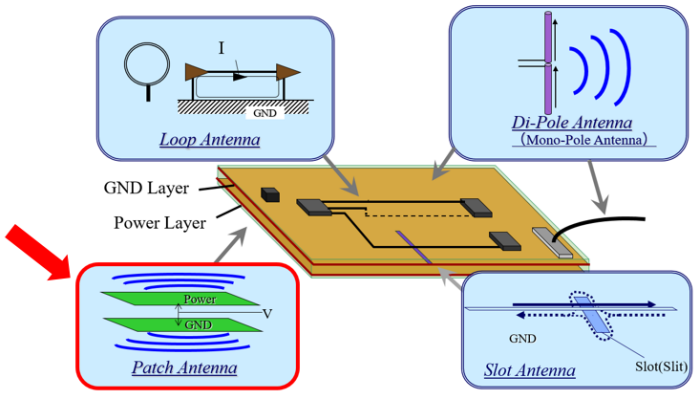
1. Improves design quality (reduces resonance between the Power and GND)
2. Reduces design costs (by arranging no more capacitors than necessary)
3. Meets product delivery dates (reduce rework arising from failures in EMC testing)

In particular, this tool is essential for designing printed circuit boards that contain highspeed digital circuits.

Issues at Design Sites

Recently, design has become more complicated due to higher-speed circuits. This has led to frequent EMI problems.
Some printed circuit boards have patterns with antenna structures not intended by their designers. Among such boards, resonance between the Power and GND is one of the dominant factors causing EMI.
When the resonance frequency and noise source frequency match, significantly high electrical intensity is observed in the far field.
Capacitors are arranged to reduce resonance between the Power and GND. As it is not realistic to use electromagnetic field simulation for verification during the design flow, capacitors may be placed at intervals of one every several tens of millimeters based on the design rules. In this case, it is impossible to adequately consider capacitor arrangement based on the board's characteristics (Power-GND pattern shape, distance and material between the Power and GND). On the one hand, insufficient capacitor arrangement causes an EMI problem, whereas excessive capacitor placement increases the production cost.

Various Antennas in PCB



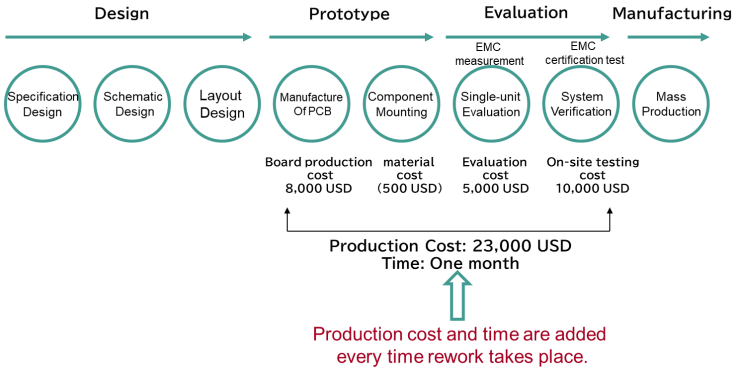
Issues

- EMI problems caused by Power-GND resonance
- Consideration of necessary and sufficient capacitor arrangement
- Higher cost due to placing excessive capacitors based on the design rules

In addition, when a PCB fails the EMC test during the evaluation phase after prototyping, it is necessary to go all the way back to the PCB Layout Design or Schematic Design to take EMI countermeasures. Longer TAT caused by rework generates problems such as failure to meet product delivery dates, lost opportunities for product sales, and increasing countermeasure costs.

As such, EMI countermeasures need to be front-loaded in the design flow.

◆ Case of rework on a 6-layer PCB

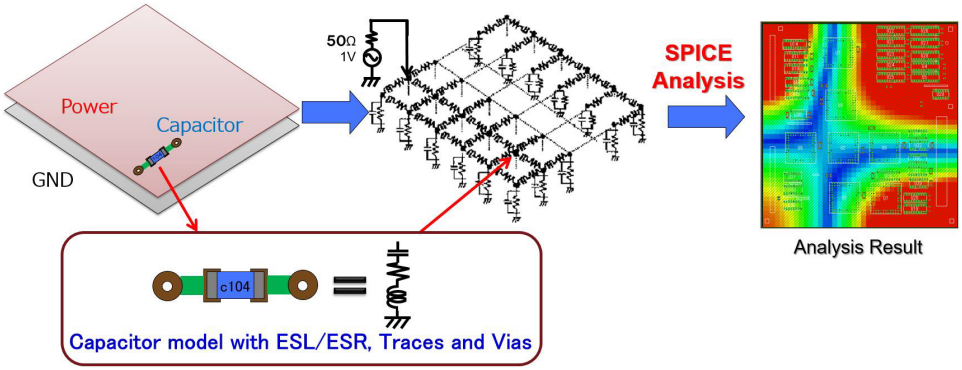


Characteristics of EMIStream Power-GND Plane Resonance Analysis

EMIStream Power-GND Plane Resonance Analysis enables you to front-load EMI countermeasures in the design phase. Using Power-GND Plane Resonance Analysis function makes it easy to avoid EMI problems caused by Power-GND resonance and consider an optimal capacitor arrangement.

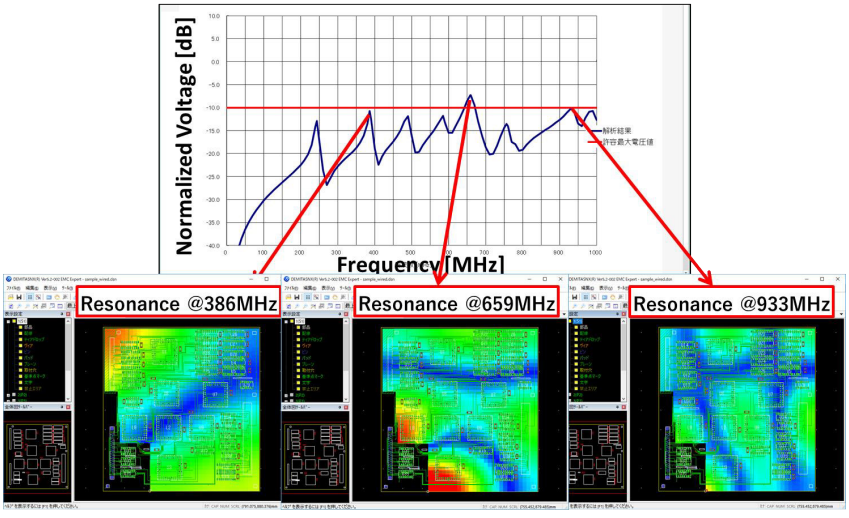
High-speed analysis engine and high analysis accuracy

The Power-GND Plane Resonance Analysis function models the Power and GND to SPICE's equivalent circuit and analyzes it by using a frequency axis. This can obtain an analysis result in 1 to 10 minutes. The function can obtain highly accurate analysis results by solving an analysis model that has tuned the skin effect and dielectric loss at each frequency, including capacitor ESL/ESR with pulling out traces.



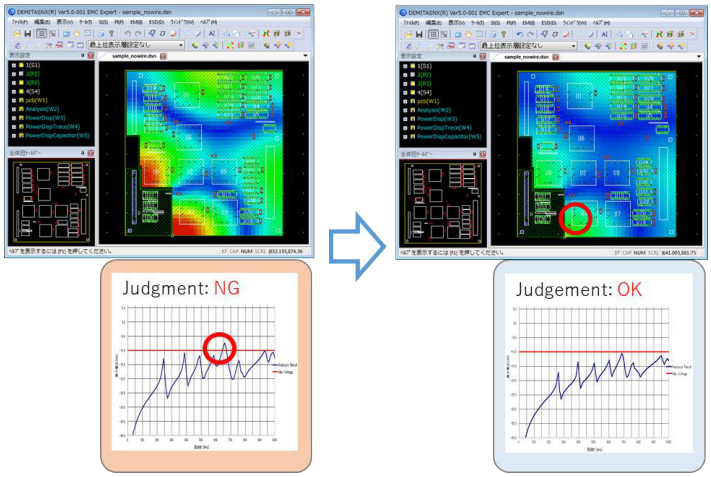
Visualization of Power-GND resonance

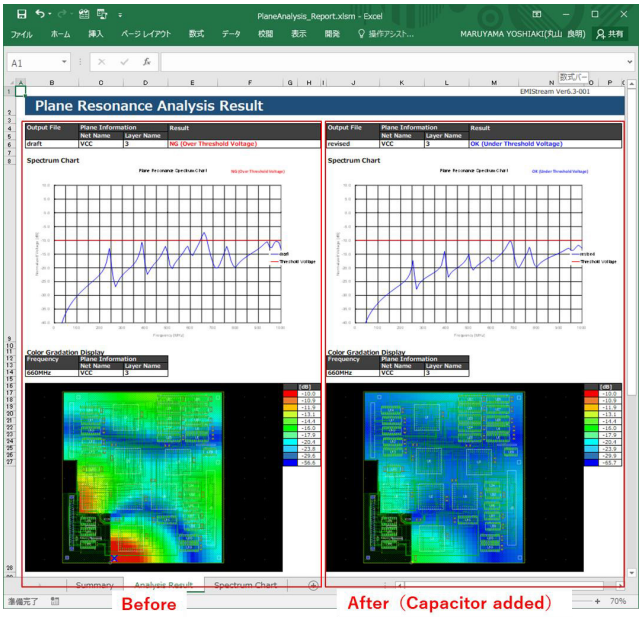
After analysis, you can see the voltage level at each frequency. By displaying the voltage distribution at frequencies with particularly high voltage levels on the layout screen, it is possible to visually check the loop and nodes of the resonance.



Simple countermeasures for resonance

Adding a capacitor to a resonance loop makes it easy to take measures against resonance. Placing enough capacitors to suppress the resonance level makes it possible to study what capacitor arrangement is necessary and sufficient.





Report of analysis results

The analysis results can be output in Excel format. Analysis conditions, judgment results, a graph of frequency and voltage level, voltage distribution gradation displays, and a list of capacitors can be reported. You can use the report as evidence of the design or in correction instructions for layout designers.

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